	the Paperwork Re	eduction /	Act of 1995, no persons a	. U.S. Pater re-reguland to respond to a collectio	PTO/SB/08B (08-03) Approved for use through 07/31/2008. ONB 0851-0031 It and Trademark Office; U.S. DEPARTMENT OF COMMERCE In of Information unless it contains a valid OMB control number.
	Lite for form 1449/PTO				Complete if Known
			•	Application Number	10/708,268
			SCLOSURE	Filing Date	02/20/2004
ST	ATEMENT	BY A	PPLICANT	First Named Inventor	Praveen K. Samudrala
	(Use as many ah	eete ee	naces send	Art Unit	2816_2914
				Examiner Name	Unassigned
Sheet	1	ø	1	Attorney Docket Number	1372.136.PRC

Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the initials. Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), votume-issue number(s), publisher, city and/or country where published. SAMUDRALA, PRAVEEN KUMER ET AL., Selective Triple modular Redundancy for SEU Mitigation in FPGAs, pgs 1-3, Ao date SAMUDRALA, PRAVEEN K. ET AL., Selective Triple Modular Redundancy (STMR) Based Single Event Upset (SEU) Tolerant Synthesis for FPGAs, pgs 1-26, Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31. ZW CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0). CARMICHAEL, CARL, Single-Event-Effect Mitigation from a System Perspective, IEEE Transactions on Nuclear Science, April 1996, 46-2, 11.650-6			NON PATENT LITERATURE DOCUMENTS	
Redundancy for SEU Mitigation in FPGAs, pgs 1-3, Ao date SAMUDRALA, PRAVEEN K. ET AL., Selective Triple Modular Redundancy (STMR) Based Single Event Upset (SEU) Tolerant Synthesis for FPGAs, pgs 1-26, SAMUDRALA, PRAVEEN K. ET AL., A Novel Technique for SEU No Mura Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31. CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0). LABEL, KENNETH A, ET Al., Single-Event-Effect Mitigation from a Syntam			the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue	T ²
SAMUDRALA, PRAVEEN K. ET AL., Selective Triple Modular Redundancy (STMR) Based Single Event Upset (SEU) Tolerant Synthesis for FPGAs, pgs 1-26, SAMUDRALA, PRAVEEN K. ET AL., A Novel Technique for SEU No Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31. CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0).	oc	1	SAMUDRALA, PRAVEEN KUMER ET AL., Selective Triple modular Redundancy for SEU Mitigation in FPGAs, pgs 1-3, no date	
Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31. CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0). LABEL, KENNETH A. ET Al., Single-Event-Effect Mitigation from a System.	DC	2	SAMUDRALA, PRAVEEN K. ET AL., Selective Triple Modular Redundancy	
Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0). LABEL KENNETH A ET Al. Single-Event-Effect Mitigation from a System	De	3	SAMUDRALA, PRAVEEN K. ET AL., A Novel Technique for SEU No Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31.	in4
LABEL, KENNETH A. ET AL., Single-Event-Effect Mitigation from a System Perspective, IEEE Transactions on Nuclear Science, April 1996, 46-2, Pp.657-6	OC	4	CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0).	
	DC	5	LABEL, KENNETH A. ET AL., Single-Event-Effect Mitigation from a System Perspective, IEEE Transactions on Nuclear Science, April 1996, 46-2, Pp. 656	-660
	·			

Examiner		Date	
Signature	N NI W		(2/) 9/21-
Offiginia	Day a. Co	Considered	1 / 6//02
FYAMINED. I	Hat Hasfaceas accordance whether an art street at the		

"EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique cliation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is ettached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

	SIPE	r
13	18 200 E	
B	Use the P	90

Sheet 1

PTO/SB/08A (08-03)
Approved for use through 07/31/2008, QMB 0651-0031
S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE the Patenwork Reduction Act of 1995, no persons are required to respond to a coffection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Application Number 10/708,268

Filing Date 02/20/2004

First Named Inventor Praveen K. Samudrala

Art Unit 2846 — My

Examiner Name Unassigned

Attorney Docket Number 1372.136.PRC

Complete if Known

Examiner Cite Document Number Publication Date Name of Patentee or Pages Colu							
initials*	Cite No.		Number-Kind Code ^{2 (Florate})	MM-00-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
DE	1	us-6,298,289 .	10/02/2001	Lloyd et al.			
Ac	2	US-4,964,126	10/16/1990	Musicus et al.			
		US					
		US-					
		US-					
		US-					
		US-			 		
		US-					
		US-					
		US-			 		
		US-		·	-		
	-+	US-					
	- 	US-					
		US-					
		US-					
		US					
	1	US-					
		US-					
 -		US-					

Examiner Initiats*	Cto 75.	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages	T
		Country Code ³ Number ^a "Kind Code ³ (# Inown)	MON-DD-YYYY		Or Relevant Figures Appear	T
						-

Examiner Signature Signature Considered 12/28/0K

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not if conformance and not considered, include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional). See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the Individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08B (08-03)

Under the Paperwork Reduction Act of 1995, no persons a	U.S. Pate	Approved for use through 07/31/2006. OMB 0651-0031 and Trademark Office; U.S. DEPARTMENT OF COMMERCE on of Information unless it contains a valid OMB control number.	
balitute for form 1449/PTO	Complete If Known		
	Application Number	10/708,268	
FORMATION DISCLOSURE	Filing Date	02/20/2004	
TATEMENT BY APPLICANT	First Named Inventor	Praveen K. Samudrala	
(Use as many sheets as necessary)	Art Unit	2816- 2919	
	Examiner Name	Unassigned	

Attorney Docket Number

1372.136.PRC

Sheet

2

of

Examiner Initials*	Cite No.	NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS) title of the artists (i.e.	
, , , , , , , , , , , , , , , , , , ,		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DC	1	EDUARDO AUGUSTO BEZERRA ET AL., Improving Reconfigurable Systems Reliability by Combining Periodical Test and Redundancy Techniques: A Case Study, IX	1-10
DC	2	ZOLTAN MEGGYESI ET AL., FPGA Design in the Presence of Single Event Upsets, CERN, Geneva, Switerland. Pp. 1-4, No date	
DC	3	Single Event Upset (SEU) Mitigation by Virtual Triple Modular Redundancy (TMR) in Design Reduces Manufacturing Cost and Lowers Power, Alternative System Concepts, Inc., pg 1-7	
DC	4	EARL FULLER ET AL., Radiation Testing Update, SEU Mitigation, and Availability Analysis of the Virtex FPGA for Space Reconfigurable Computing, pg. 1-11, 9/200	Ð
DC	5	K. NIKOLIC ET AL., Fault-Tolerant Techniques for Nanocomputers, TNT2001, Sept. 3-7, 2001, Segovia, Spain, Pp. (-3	٠
AC	6	CARL CARMICHEAL ET AL., SEU Mitigation Techniques for Virtex FPGAs in Space Application, Pl. [-1], Heading 1999	1
De	_	PRAVEEN SAMUDRALA ET AL., Single Event Upsets and Mitigation Techniques: A Survey, pages 1-15, no date.	
DC	8	SRINIVAS KATKOORI, SEU Tolerant Design Techniques for Space Based RC Implementations, IR & D Project, March 28, 2001, Pri - 2	
OC.	9	PRAVEEN K. SAMUDRALA, Synthesis of SEU Tolerant FPGAs, January 22, 2003, pages 1-53.	

Examiner	a //	111		
Signature	13. 1		Date	12/29/20
	Ned if reference considered with		Considered	1701/04
considered, inch	ude copy of this form with next or	her or not citation is in conformance wit immunication to applicant.	h MPEP 809. Draw line through ci	tetion if not in conformance and not

1 Applicant's unique citation designation number (optional). 2 Applicant is to piece a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will very depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:

If you need assistance in completing the form, cell 1-800-PTO-9199 (1-800-785-9199) and select option 2.